REMARKS

Claims 1-7, 15-26, and 30-35 are pending. Claims 1, 15, and 19 are in independent form.

Rejections under 35 U.S.C. § 103(a)

In the Office action mailed March 13, 2008, claim 1 was rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,933,627 to Parady (hereinafter "Parady") and U.S. Patent No. 5,787,454 to Rohlman (hereinafter "Rohlman").

Claim 1 relates to an execution unit for execution of multiple context threads. The execution unit includes an arithmetic logic unit to process data for executing threads, control logic to control the operation of the arithmetic logic unit, and a general purpose register set to store and obtain operands for the arithmetic logic unit.

The register set includes a plurality of two-ported random access memory devices assembled into banks. The register set includes two effective read ports and one effective write port. The effective write port includes write ports of a pair of the two-ported random access memory devices. Each bank is capable of performing a read and a write to two different words in the same processor cycle. The arithmetic logic unit can write to each bank in the general purpose register set using the one effective write port.

The rejection of claim 1 is based on the contention that "Parady was relied upon to teach '… the register set comprising a plurality of two-ported random access memory devices assembled into banks (Parady 48 of Fig.1/Fig.3), each bank being capable of performing a read and a write to two different words with two ports in the same processor cycle…'" *See, e.g., Office action mailed March 13, 2008*, page 13, para. 38. *See also id.*, page 3, para. 7, c.

Applicant respectfully disagrees. Indeed, upon review of the prosecution, Applicant has remarked on this disagreement many times. For example, in the Response filed February 17, 2006, Applicant remarked that,

> "[i]n regard to Parady, the rejection contends that Parady's integer registers 48 constitute a register set that comprises a plurality of two-ported random access memory devices. However, Paraday is silent as to the architecture of integer registers 48. Indeed, integer registers 48 appear to be standard registers with hardware ports as shown in FIG. 1. Certainly nothing about Parady's registers describes or suggests that integer registers 48 comprise a plurality of two-ported random access memory devices.
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> Indeed, the only mention of two-ported register files made in Parady is found at col. 5, line 30-43. In this section, Parady acknowledges that multi-ported register files can occupy more silicon that simple duplication of registers. However, the duplication of dual ported register files described by Parady does not suggest a register set that comprises a plurality of two-ported random access memory devices and that includes two effective read ports and one effective write port. For example, FIG. 7

> illustrates how Parady envisages dual ported register files can be duplicated. In particular, dual ported shadow registers 186 are to be individually addressed using a data switch 192 or individually enabled for writing along a path 194. Such individual addressing or individual enablement does not provide a register set that comprises two-ported random access memory devices and includes two effective read ports and one effective write port, as recited in claim 1. Rather, individual addressing or individual enablement of a dual ported register file inherently limits the effective ports to two-- i.e., the two ports on the individually addressed or individually enabled dual ported register file." *See Response filed February 17, 2006*, page 10-11.

As best understcod before the mailing of the March 13, 2008 Office action, this position was accepted by the Examiner when raised. *See Advisory Action mailed March 27, 2006* (relying upon the publication entitled "Computer Systems Design and Architecture" by Heuring and Jordan to show two-ported random access memory devices).

Applicant maintains this position. Indeed, this position was reiterated in the response filed December 11, 2007. *See Response filed December 11, 2007*, page 14, line 3-5 (pointing out that Paraday is silent as to the architecture of integer registers 48 and thus also fails to describe or suggest that two-ported random access memory devices be assembled into the recited banks).

Applicant respectfully requests that the Examiner identify with specificity if and why the Examiner persists in believing that Parady's integer registers 48 comprise a plurality of two-ported random access memory devices assembled into banks.

In the absence of any grounds for believing that Parady's integer registers 48 comprises a plurality of two-ported random access memory devices assembled into banks, Applicant reiterates the Remarks regarding Rohlman set forth in the Response filed December 11, 2007. In particular, Rohlman's cells are each capable of storing a single bit, reading a single bit, and writing a single bit. Rohlman's cells are thus not capable of performing a read and a write to two different words, much less two different words in a same processor cycle, as recited of each bank in claim 1. There is nothing in Rohlman that describes or suggests how to assemble Rohlman's cells into the recited banks.

Further, the banks in Rohlman's Re-Order Buffer (ROB) also do not constitute the recited banks. In this regard, Rohlman makes it clear that each data input 412, 414, 416, 418 allows data input to a single bank. None of data inputs 412, 414, 416, 418 can be used to write to each of the multiple banks in Rohlman's Re-Order Buffer (ROB).

Thus, the qualities ascribed to Paraday's integer registers 48 in the rejection (e.g., each bank being capable of performing a read and a write to two different words in the same processor cycle) are not present in any bank assembled from a plurality of two-ported random access memory devices. Indeed, Rohlman's cells and Re-Order Buffer appear to be excluded from performing the recited limitation, and Parady requires standard registers to achieve the recited limitation.

Thus, even if Paraday and Rohlman were combined, one of ordinary skill would not arrive at the recited subject matter. Accordingly, claim 1 is not obvious over Paraday and Rohlman. Applicant respectfully requests that the rejections of claim 1, and the claims dependent therefrom, be withdrawn.

Claim 15 was rejected under 35 U.S.C. § 103(a) as obvious over Parady and Rohlman.

Claim 15 relates to a method for executing multiple context threads. The method includes processing data for executing threads within an arithmetic logic unit, operating control logic to control the arithmetic logic unit, and storing and obtaining operands for the arithmetic logic unit within a general purpose register set comprising a plurality of banks of two-ported random access memory devices.

The register set includes two effective read ports and one effective write port. The effective write port comprises write ports of a pair of the two-ported random access memory devices. The effective write port includes a single write line to write to addresses in different banks of the plurality of banks. Each bank is capable of performing a read and a write to two different words in the same processor cycle.

The rejection of claim 15 is understood to be based on the same contention discussed above, namely, the contention that Parady's integer registers 48 constitute a register set that comprises a plurality of two-ported random access memory devices. Applicant disagrees and respectfully requests that the basis for this contention be stated.

In the absence of any grounds for believing that Parady's integer registers 48 comprises a plurality of two-ported random access memory devices, Applicant reiterates the Remarks regarding Rohlman set forth in the Response filed December 11, 2007 and submits that, even if Paraday and Rohlman were combined, one of ordinary skill would not arrive at the recited subject matter.

Claim 15 is thus not obvious over Paraday and Rohlman. Applicant respectfully requests that the rejections of claim 15, and the claims dependent therefrom, be withdrawn.

Claim 19 was rejected under 35 U.S.C. § 103(a) as obvious over Parady and Rohlman.

Claim 19 relates to a processor unit that includes an execution unit for execution of multiple context threads. The execution unit includes an arithmetic logic unit to process data for executing threads, control logic to control the operation of the arithmetic logic unit, a general purpose register set to store and obtain operands for the arithmetic logic unit, and a data link between the arithmetic logic unit and the one effective write port of the general purpose register set.

The register set includes a plurality of two-ported random access memory devices. The register set comprising two effective read ports and one effective write port. The effective write port comprises write ports of a pair of the two-ported random access memory devices. The data link allows the arithmetic logic unit to write to different two-ported random access memory devices in the general purpose register set through the one effective write port.

The rejection of claim 19 is based on the contention that Parady's integer registers 48 are a register set that includes a plurality of two-ported random access memory devices, as recited in claim 19. See Office action mailed March 13, 2008, paragraph iii bridging page 6-7 (contending that Parady's integer

registers 48 are a general purpose register set comprising a plurality of two-ported random access memory devices).

Applicant respectfully disagrees and respectfully requests that the basis for this contention be stated.

In the absence of any grounds for believing that Parady's integer registers 48 comprises a plurality of two-ported random access memory devices, Applicant reiterates the Remarks regarding Rohlman set forth in the Response filed December 11, 2007 and submits that, even if Paraday and Rohlman were combined, one of ordinary skill would not arrive at the recited subject matter.

Claim 19 is thus not obvious over Paraday and Rohlman. Applicant respectfully requests that the rejections of claim 19, and the claims dependent therefrom, be withdrawn.

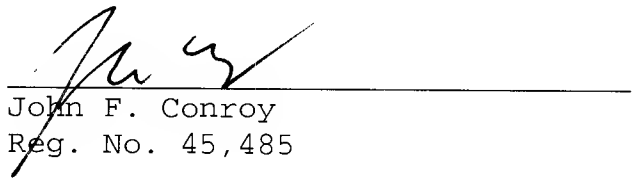
It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as

specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicant asks that all claims be allowed. No fees are believed due at this time. Please apply any charges or credits, to Deposit Account No. 06-1050.

Respectfully submitted,

Date: May 5, 2008



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